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Randomized instruction set emulation [PDF] from psu.edu
EG Barrantes, DH Ackley, S Forrest, ... - ACM Transactions on ..., 2005 - portal.acm.org
... 4.1 Possible Behaviors of Random Byte Sequences First, we characterize the possible events associated with a generic processor or emulator attempting to execute a ... (1) A symbol is a string of l bytes, which may or may not belong to the in- struction set. ... (2) An **instruction** is a ...
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Multiscalar processors [PDF] from psu.edu
GS Sohi, SE Breach, ... - Proceedings of the 22nd ..., 1995 - portal.acm.org
... to the set of values that may be consumed by the task and the set of values that ... In a sequential exe- cution, the information is discovered during the **instruction** decode process as instructions are ... of the CFG is performed by the com- piler to supply the create **mask** that indicates ...
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RISC I: A reduced instruction set VLSI computer [PDF] from psu.edu
DA Patterson, ... - 25 years of the international symposia ..., 1998 - portal.acm.org
... by Y. Tamir. RISC I **simulator** BY R. Campbell, E. Lock, and M. Hakam: RISC I **simulator** by Y ... The case for the reduced **instruction set** computer, Computer Architecture News, 8 (15 Oct. ... The Potible C Compiler for the VAX c2 CIFPLOT - a program that plots **VLSI mask** layouts on ...
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Hybrid-compiled simulation: An efficient technique for instruction-set architecture simulation [PDF] from psu.edu
M Reshadi, P Mishra, ... - ACM Transactions on Embedded ..., 2009 - portal.acm.org
... The decoding step during runtime consults the **mask** table and determines the ... use traditional interpretive techniques for executing modified instructions while the **instruction-set** compiled technique ... In static-compiled simulation, the generated **simulator** is optimized by the C++ ...
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Reduced instruction set computing apparatus and methods
GA Portanova, ... - US Patent 4,992,934, 1991 - Google Patents
... a 16-bit status S word (SW), a 16-bit **instruction** counter (IC), a 16-bit **mask** register (MK ... aspect of the present inven- tion, the RISC is designed for use as an emulator of a ... The "reduced" **instruction set** dis- closed in the specification is particularly well suited for execution on the ...
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Reducing the performance impact of instruction cache misses by writing instructions into the reservation stations out-of-order
J Stark, P Racunas, ... - Proceedings of the 30th annual ACM ..., 1997 - portal.acm.org
... interpreter (python), version 2.0 of the SimpleScalar superscalar out-of-order execution processor **simulator** (ss), and ... The configuration of the **instruction** cache given above is its default configuration. In our experiments, we will vary its **set** associativity, its size, and its miss latency ...
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An architectural framework for supporting heterogeneous instruction-set architectures [PDF] from psu.edu
OM Stoerman, ... - Computer, 2002 - ieeexplore.ieee.org
... IBM TJ Watson Research Center A novel architectural framework allows applications written for one **instruction set** to migrate to a higher performance architecture without a significant investment by the user or developer. ... **Instruction-set** migration ...
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Dynamic hammock predication for non-predicated instruction set architectures [PDF] from psu.edu
A Klauser, T Austin, D Grunwald, ... - Parallel Architectures ..., 2002 - ieeexplore.ieee.org
... Thus the dynamic scheduler can trivially determine that instructions outside of the predicate ... **instruction** specified the predi- cation information for subsequent instructions using a bit-**mask**. ... full predication in the microar- chitecture without requiring additional **instruction set** support ...
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Trace cache: a low latency approach to high bandwidth instruction fetching [PDF] from psu.edu
E Rotenberg, S Bennett, ... - ... of the 29th annual ACM/IEEE ..., 1996 - portal.acm.org
... If the trace does not end in a branch, the target address is **set** equal to the fall-through address. ... SPARC **instruction** traces were gener- ated using the Quick Profiler and Tracer (QPT) [7] and then fed into the trace-driven SPARC processor **simulator**. ...
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Cyclone: a broadcast-free dynamic instruction scheduler with selective replay [PDF] from psu.edu
E Ernst, A Hamel, ... - Computer Architecture, 2003. ... 2003 - ieeexplore.ieee.org
... in this study are derived from the SimpleScalar/Alpha version 3.0 tool **set** [2], a ... The timing **simulator** executes only user-level instructions, performing a detailed timing simu- lation of an aggressive dynamically scheduled micropro- cessor with two levels of **instruction** and data ...
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ISDL: An **instruction set** description language for **retargetability** [PDF] from psu.edu
G Hadjiyiannis, S Hanono, ... - 1997 - computer.org
... to a binary file that is used as input to the **Instruction** Level **Simulator** (ILS). ... MIMOLA is too low level for **retargetable** compilers, and it does not support the definition of ... In particular, it includes an **instruction set** description, a listing of the available resources, and an interconnect ...
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ISDL: An instruction set description language for **retargetability** and architecture exploration
G Hadjiyiannis, S Hanono, ... - Design Automation for ..., 2000 - Springer
... Support the automatic generation of a cycle-accurate **instruction** level **simulator**. • Support the automatic generation of a hardware model. ... Section 6 presents previous work on **retargetability** and machine description languages. ... **INSTRUCTION SET** DESCRIPTION LANGUAGE ...
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[PDF] Aviv: A **Retargetable** Code Generator for Embedded Processors [PDF] from psu.edu
SZ Hanono - 1999 - Citeseer
... executed in parallel. The third step of the compilation process is to select a **set** of target processor ... The Aviv **retargetable** code generator is one element of a software synthesis system ... Once the code has been generated, an **instruction**-level **simulator** analyzes the generated ...
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Automatic checking of **instruction** specifications [HTML] from hrlb.edu
M Fernandez, ... - ... of the 19th international conference on ..., 1997 - portal.acm.org
... generated from our specifications has been used in our own **retargetable** de- bugger [22] and **retargetable**, optimizing linker [S ... 0, eg, Bicc is bound to op = 0 ti op2 =I 2. Bindings to the **wildcard** I\" are ... Many assemblers extend the real **instruction set** with "syn- thetic" instructions. ...
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[PDF] Automatic checking of **instruction** specifications [PDF] from psu.edu
N Ramsey - 1997 International Conference on Software ..., 1997 - Citeseer
... generated from our speci cations has been used in our own **retargetable** de- bugger 22] and **retargetable**, optimizing linker ... op = 0, eg, Bicc is bound to op = 0 & op2 = 2. Bindings to the **wildcard** _" are ... Many assemblers extend the real **instruction set** with \syn- thetic" instructions. ...
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[BOOK] High-level synthesis for real-time digital signal processing
J Vanhoof - 1995 - books.google.com
... Dui69] and MIMOLA [Zim76]. Depending on the abstraction level, a behavioural speification of a computer is either a register-transfei descrption 01 a description of the **instruction set** of the machine. • **ALERT** and the **DDL** compiler ...
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Specifying representations of machine instructions [PDF] from psu.edu
N Ramsey,... - ACM Transactions on Programming ..., 1997 - portal.acm.org
... ldb [Ramsey 1992; Ramsey and Hanson 1992], a **retargetable** debugger, uses the toolkit to decode ... 1, and Bicc is bound to op = 0 & op2 = 2. Bindings to the **wildcard** " " are ignored. ... For example, the synthetic **instruction set** [SPARC International 1992, p. 84] expands to a single ...
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Visualisation as an aid to low-level programming [PDF] from fie-conference.org
M Beaumont, ... - ... Teaching and Learning in an Era ..., 2002 - ieeexplore.ieee.org
... access and manipu- late data is often neither straightforward nor consis- tently applied throughout the **instruction set**. ... However, as we intend our system to be **retargetable** we have incorporated this into our ... a glance which addressing modes are appropriate to any **instruction**. ...
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[PDF] Norman Ramsey, Purdue University Mary F. Fernandez, Princeton Universitvy December 12, 1995 [PDF] from psu.edu
MF Fernandez - 1995 - Citeseer
... ldb (Ramsey 1992; Ramsey and Hanson 1992), a **retargetable** debugger, uses the toolkit to ... The **wild-card** constraint 'some class" matches any token of class class, for example, on the ... de nitions helps a speci cation writer organize the description of a machine's **instruction set**. ...
Related articles - View as HTML - All 2 versions

Case studies on automatic extraction of target-specific architectural parameters in complex code generation
Y Fiser, M Ami - Software and Compilers for Embedded Systems, 2003 - Springer
... 2 4 Fig. 1. The matching process: The symbol i represents an integer constant, and the symbol ra **wildcard** variable that can match any symbol. ... the input for r . Another architectural factor that contributes curtailing the DAG search time for ARM9 is its RISC-like **instruction set**; that is ...
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... When reading the machine program, each **instruction** is decoded, ie, the **set** of RTs to be simulated in the current **instruction** are determined. De- pending on the selected simulation mode (interpretive or **compiled**), decoding takes place at simulation time or **simulator** ...
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... The **simulator** recognizes if the previously decoded **instruction** has changed and initiates re-decoding of the modified **instruction**. If any **instruction** 759 Page 3. ... Customized Inst. **Template** C++ Compiler ... Program Decoded Figure 3: **Instruction Set Compiled** Simulation Flow ...
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Compiled instruction set simulation [PDF] from psu.edu
C Mills, SC Ahalt, ... - Software: Practice and ..., 1991 - interscience.wiley.com
... A **macro** assembler might do a better job of translating certain architectures (ie ones with flags), but at a significant loss of portability. ... Consequently, **compiled instruction simulators** are best used as an efficient **instruction set** prototyping tools. ...
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D Burger, ... - ACM SIGARCH Computer Architecture News, 1997 - portal.acm.org
... We provide pre- **compiled** test binaries (big- and little-endian) and their sources in SIDR/simplesim2.0/tests). ... **macro** definition for each **instruction** in the **instruction set**. ... The **instruction** actions (which appear as macros) that are common to all **simulators** are defined in --sh Those ...
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SSIM: a software levelized compiled-code simulator [PDF] from psu.edu
LT Wang, NE Hoover, EH Porter, ... - Proceedings of the 24th ..., 1987 - portal.acm.org
... six benchmarked circuits running on an Apollo DN570-T 32-bit workstation (with **instruction** cache ... For the last four circuits, time to **set** input patterns had been reduced to a ... 5. SUMMARY AND CONCLUSIONS A logic simulation technique using levelized **compiled**- code (LCC) for ...
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M Reshadi, N Bansal, P Mishra, ... - ... of the 1st IEEE/ACM/IFIP ..., 2003 - portal.acm.org
... in ARM, described in Figure 4. /* extracted **template** for data processing operations of ARM*/ **template**<class Conditions ... EXPRESSION: A Language for Architecture Exploration through Compiler/**Simulator** Retargetability ... [2] M.Reshadi et al, **Instruction-Set Compiled** Simulation: A ...
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A Hoffmann, T Kogel, A Nohl, ... - ... -Aided Design of ..., 2002 - ieeexplore.ieee.org
... The interpretive **simulator** is not discussed. 1) **Compiled** Simulation: The objective of **compiled** simula- tion is to reduce the simulation time. Considering **instruction-set** simulation, efficient runtime reduction can be achieved by per- forming repeatedly executed operations only ...
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Improvement of compiled instruction set simulator by increasing flexibility and reducing compile time [PDF] from psu.edu
MF Chung, ... - Rapid System Prototyping, 2004. ..., 2004 - ieeexplore.ieee.org
... code with **instruction** abstraction technique, which classifies instructions using C++ **template** to improve ... 2003 [2] Jianwen Zhu, Gajski DD, "An ultra-fast **instruction set simulator**", VLSI Systems ... M., Dutt N., "Reducing compilation time over- head in **compiled simulators**", 21st ICCD ...
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[BOOK] Evaluating future microprocessors: The simplescalar tool set [PDF] from psu.edu
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... The version.h include file is built when the Linux kernel is **compiled**. ... architecture is defined in ss.def, which contains a **macro** definition for each **instruction** in the **instruction set**. ... The **instruction** actions (which appear as macros) that are com- mon to all **simulators** are defined in ss ...
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A methodology for the design of application specific instruction set processors (ASIP) using the machine description language LISA [PDF] from wtb.tue.nl
A Hoffmann, O Schliebusch, A Nohl, G Braun, ... - 2001 - computer.org
... Besides the ability to generate a complete **set** of software de- velopment tools, synthesizable HDL code for the processor's control path and **instruction** decoder can ... generated simu- lation tools are enhanced in speed by applying the **compiled** simulation principle ...
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B Cmelik, ... - Proceedings of the 1994 ACM SIGMETRICS ..., 1994 - portal.acm.org
... Page 4. Translations for conditional branches are **compiled** with two **...** The TLB is an array of lists of <target, host> address pairs. Each pair associates an application **instruction** address with the **...** The TLB may also be thought of as N-way **set** associative, where N is the list length. **...**
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... 4.1 Experimental Setup The ARM7 processor is a RISC machine with fairly com- plex **instruction set ...** The generated **simulator** code is **compiled** using the Microsoft Vi- sual Studio .NET compiler **...** used these two bench- marks to be able to compare our **simulator** performance with **...**
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... less effort has been spent so far on retar- getable **instruction set simulators**, which are **...** program for a fixed application program, thereby mov- ing the **instruction** decoding overhead to **...** While the **compiled** approach achieves significantly higher speed, its disadvantage is that the **...**
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A retargetable, ultra-fast **instruction set simulator** [PDF] from psu.edu
J Zhu, DD Gajski - Design, Automation and Test in Europe ..., 2002 - ieeexplore.ieee.org
... which uses a vir- tual machine code generation interface for the static **compiled** ISA simulation. **...** retargetable, as our experience show that porting an ISA **simulator** to a new host **...** Our future work will extend this methodology to perform cycle accurate **instruction set** simulation, and **...**
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Compiled HW/SW co-simulation
V Zivojnovic, ... - Proceedings of the 33rd annual Design ..., 1996 - portal.acm.org
... [3] S. Sutarwala, P. Paulin, and Y. Kumar, Insulin: An **instruction set** simulation environment," in Proc. **...** [4] Z. Barzilai, et al., IHSS - A high speed **simulator**," IEEE Trans. **...** [7] V. Zivojnovi c, S. Tjiang, and H. Meyr, "**Compiled** simulation of programmable DSP architectures," in Proc. **...**
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Compiled simulation of programmable DSP architectures
V Zivojnovic, S Tjiang ... - The Journal of VLSI Signal Processing, 1997 - Springer
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... the time-to- market pressure, simulation speed is the most impor- tant factor in **instruction set** simulation. **...** for the partial modification of the target software, user should go through all the **simulator** generation processes. **...** Second, the static **compiled** ISS has restrictions on flexibility. **...**
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MR Hartoog, JA Rowson, PD Reddy, S Desai, ... - 1997 - computer.org
... The **compiled instruction set simulator** [8] decodes a program and generates a model for that program running on a processor. This has obvious restrictions, such as no **self modifying** code, but because the decode is done once at model generation time, it pro- duces models that **...**
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The Transmeta Code Morphing™ Software: using speculation, recovery, and adaptive retranslation to address real-life challenges [PDF] from psu.edu
JC Dehnert, BK Grant, JP Banning, ... - ..., 2003. CGO 2003. ..., 2003 - ieeexplore.ieee.org
... In addition, a given x86 **instruction** can access both regular memory and I/O space **...** representative subset of the results, along with the means for the entire **set** (see Appendix **...** Although these are becoming less common in modern **compiled** applications, device drivers, games like **...**
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... from disk, or be encoded and copied into a completely dis- joint **set** of memory **...** prefetch block so that further processing can proceed normally in actually decoding the correct **instruction. ...** Periodically re-randomizing programs (eg, when the system is re-**compiled** for open-source **...**